WHAT IS CLAIMED IS:

1. A method for producing yield enhancement data for integrated circuits on a substrate, the method comprising the steps of:

comparing a database of defects on the substrate to a database of design information for the integrated circuits, and

associating the defects on the substrate with classes of design information to produce the yield enhancement data.

2. The method of claim 1, wherein the database of defects comprises a defect wafer map.

3. The method of claim 1, wherein the defects on the substrate are optically observable defects.

4. The method of claim 1, wherein the design information includes structures formed in the integrated circuits.

5. The method of claim 1, wherein the classes of design information comprises classes of physical structures.

6. The method of claim 1, further comprising the step of creating the database of defects by inspections of the substrate, where the inspections are conducted at multiple times during fabrication of the integrated circuits.

7. The method of claim 1, further comprising the step of creating the database of design information from design files for the integrated circuits.

8. The method of claim 1, further comprising the step of revising the design information based at least in part on the yield enhancement data.

9. A method for producing yield enhancement data from integrated circuits on a substrate, the method comprising the steps of:

creating a database of design information for the integrated circuits, which design information is used as a template for fabricating the integrated circuits,

creating a database of defects on the substrate during processing of the integrated circuits,

comparing the database of design information with the database of defects to create associations between the design information and the defects, and

associating the database of defects with the database of design information by physical proximity of the defects to classes of the design information to produce the yield enhancement data.

10. The method of claim 9, wherein the database of defects comprises a defect wafer map.

11. The method of claim 9, wherein the defects on the substrate are optically observable defects.

12. The method of claim 9, wherein the design information includes structures formed in the integrated circuits.

13. The method of claim 9, wherein the classes of design information comprises classes of physical structures.

14. The method of claim 9, wherein the step of creating the database of defects comprises inspections of the substrate, where the inspections are conducted at multiple times during the fabrication of the integrated circuits.

15. The method of claim 9, further comprising the step of revising the design information based at least in part on the yield enhancement data.

16. A computerized system for analyzing defects, the system comprising:

means for receiving design information for integrated circuits, where the integrated circuits are fabricated on a substrate based on the design information,

means for receiving defect information for integrated circuits, where the defect information contains locations of defects on the substrate,

means for comparing the design information with the defect information, and

means for associating the defects with classes of the design information based on physical proximity on the substrate to produce yield enhancement data.

17. The system of claim 16, wherein the defect information comprises a defect wafer map.

18. The system of claim 16, further comprising means for revising the design information based at least in part on the yield enhancement data.

19. The system of claim 16, wherein the design information includes structures formed in the integrated circuits.

20. The system of claim 16, wherein the classes of the design information include classes of structures formed in the integrated circuits.